Interfacing EXOSTIV Probe EP Series

User Guide

Rev. 2.0.9 - November 5, 2024

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References

[1] SFF committee, INF-8074i specification for SFP (Small Formfactor Pluggable) Transceiver (May 12, 2001)

Revision History

Revision	Modifications
1.0.26	• Original revision
1.0.47	• Notes added below Table 6 • HDMI I²C minimum reference level changed to +2.5V. Table updated accordingly • Notes added below Table 1 • Different minimum VREF value for GPIO lines 0-3 (**Error! Reference source not found.**) and 4-5 (+1.65V) • Pin mapping correction for GPIO connector (**Error! Reference source not found.** and **Error! Reference source not found.**) • DC characteristics for GPIO lines split in **Error! Reference source not found.** and **Error! Reference source not found.**
1.0.53	• Pin mapping for HDMI type-C added (Table 6)
1.0.115	• Extended document to cover all EP devices
2.0.0	• General review with EXOSTIV Dashboard for Intel release
2.0.1	• Corrected some typos
2.0.2	• Removed description of optical SFP cables.
2.0.3	• Update of legal and brand names. • Removed obligation to use copper cables.
2.0.4	• Corrected information about optical cables. • Removed reference to EP3000 probes.
2.0.5	• Updated the status of the 'HDMI' connector to not recommended for new designs – legacy.
2.0.6	• Description of ARF6-08 connector
2.0.7	• Added references to EP16000 Probe
2.0.8	• Removed references to deprecated I²C downstream channel using the HDMI connector
2.0.9	• Added remarks about transceiver reference clock in introduction.

Interfacing EP Series

Introduction

EXOSTIV Probe ('EP Series') device requires a bi-directional link to connect to the target system. This bi-directional link is composed of:

- a potentially lower data rate downstream link from the EP device to the target system. It is used to configure and control the IP embedded in the FPGA.
- a high-speed upstream link from the target FPGA to the EP device to collect the captured data.

The EP series devices use transceivers (or 'multi-gigabit transceivers', or 'MGT' or SERDES) to implement the upstream link.

In this document, we provide the description of several usable connectors and corresponding pinout, used to connect the Exostiv hardware to the target FPGA. When making the target FPGA board, the transceivers should be operational. Especially, the board should feature a reference clock source for the transceivers, that is generally not provided by the connectors described in this document. EP Series devices support multiple such reference clock settings – please refer to this article for an updated list of such frequencies.

In the first revision of the EP Probe devices (EP6000 and EP12000), 2 connection options are available on the probe's front panel:

- Option 1: 4 SFP/SFP+ cages able to receive passive SFP copper cables or SFP/SFP+ optical transceiver modules
- Option 2: A HDMI form factor connector type-A with up to 4 simplex multi-gigabit links.

Important note : *It is not recommended to use this option as custom connector for new designs. The description that follows is provided for legacy support purposes. From the EP16000 series probe, this connector **is not supported**. Consider using the ARF6-08 connector as replacement high-density connection option.*

The current revision of the EP probe devices (EP16000) offers two different connection options:

- Option 3: A QSFP28 cage able to receive a passive QSFP/QSFP+/QSFP28 copper cable or QSFP/QSFP+/QSFP28 optical transceiver module.
- Option 4: An ARF6-08 connector from SAMTEC. This compact form factor high speed connector gives the possibility to implement a link with up to 4 channels using a passive cable on a PCB area as small as 0.8 cm^2 (0.124 in^2).

The low data rate downstream link is implemented using either MGT or a low speed serial link similar to I^2C.

The purpose of this document is to provide the necessary information to correctly connect the EP series devices to the user's target system. Pin assignments, mechanical and electrical specifications of the connectors are provided to help designers implement interfaces compatible with Exostiv Labs devices.

The following models of EXOSTIV Probes EP series are available:

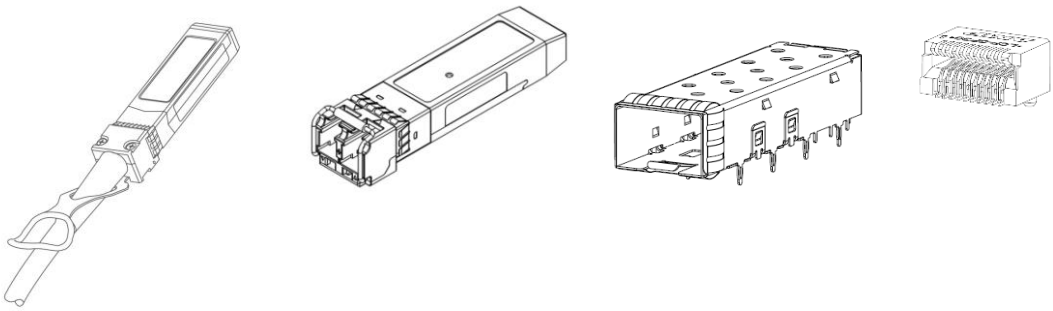
EXOSTIV Probes	EP6000	EP12000	EP16000
Max. speed per channel	6.6 Gbps	12.5 Gbps	16.25 Gbps
Number of channels (Transceivers)	1,2 or 4		4
Supported devices	Please click here.		Please click here

EXOSTIV Probe user's guide can be found on Exostiv Labs' general documentation page.

Notes:
1. *Please contact us for other devices and manufacturers support, availability and roadmaps.*
2. *FPGA devices that will be supported in the future with the EP6000, EP12000 and EP16000 probes will use the pinout described in this document.*
3. *Other probe number encoding such as EP6000-X, EP12000-X, EP6000-I or EP12000-I with 'X' or 'I' suffix are now covered by the generic numberings, 'EP6000' and 'EP12000'.*
4. *EP6000 and EP12000 are legacy products that are now discontinued, but still supported.*

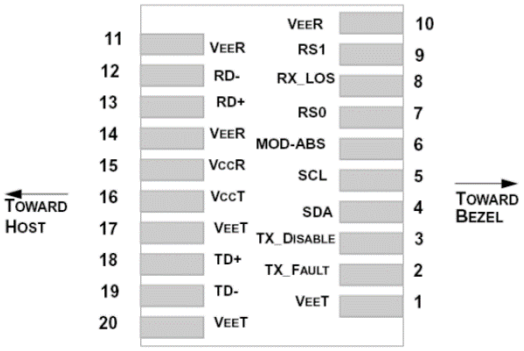
SFP/SFP+ Cages

EP series can be connected to up to 4 simplex or full-duplex multi-gigabit links through SFP/SPF+ physical interface. The SFP/SFP+ cages can receive passive cables or optical cables. The connector pin assignment is compatible with the standard proposed by the MSA group [1].



Using the SFP/SFP+ interface enables the implementation of a full-duplex link. Upstream data flow (TX) refers to data transmitted from the target system to the EP device. Downstream data flow (RX) refers to data received by the target system from the EP device.

A downstream link is mandatory to let the EP device control the IP embedded in the FPGA. A single downstream link is required, even if multiple SFP/SFP+ links are used for the upstream link.



igure 1: SFP+ receptacle pin mapping

Table 1: SFP/SFP+ connector pin assignment

Pin #	Signal	Description	Usage
1	VeeT	Transmitter ground	Mandatory
2	TX Fault	Transmitter fault indication. Open collector/drain output. 4.7K to 10K pull-up required.	Optional
3	TX Disable	Active high transmitter disable.	Optional
4	MOD-DEF2	SDA line for I²C interface. Pull-up resistor required.	Optional
5	MOD_DEF1	SCL line for I²C interface. Pull-up resistor required.	Optional
6	MOD-DEF0	Active low module presence detection. Pull-up resistor required.	Optional
7	RS0	Receiver rate select.	Optional
8	LOS	Loss of receiver signal. Open collector/drain output. 4.7K to 10K pull-up required.	Optional
9	RS1	Transmitter rate select.	Optional
10	VeeR	Receiver ground	Mandatory
11	VeeR	Receiver ground	Mandatory
12	RD-	Inverted received data out. Connect to MGTPRXN, MGTXRXN or MGTHRXN pin of the FPGA.	Mandatory[1]
13	RD+	Received data out. Connect to MGTPRXP, MGTXRXP or MGTHRXP pin of the FPGA.	Mandatory[1]
nda	VeeR	Receiver ground.	Mandatory
15	VccR	Receiver power.	Optional[2]
16	VccT	Transmitter power.	Mandatory[3]
17	VeeT	Transmitter ground.	Mandatory
18	TD+	Transmit data in. Connect to MGTPTXP, MGTXTXP or MGTHTXP pin of the FPGA.	Mandatory
19	TD-	Inverted transmit data in. Connect to MGTPTXN, MGTXTXN or MGTHTXN pin of the FPGA.	Mandatory
20	VeeT	Transmitter ground	Mandatory

[1] *If a multi-link connection is implemented, only one RD+/RD- is mandatory. Mandatory for single-link connection.*
[2] *Optional if only passive cables are used for RD+/RD-*
[3] *Optional if only passive cables are used for TD+/TD-*
[4] *Transceiver + and – signals can be swapped within a differential pair if it is required to improve the layout. The EP can dynamically invert the polarity of the received signals.*

When passive cables are used, it is not mandatory to provide power on these pins and they can be connected to GND. Please note that the internal identification EEPROM cannot be accessed if no power is provided to the SFP cable. In this case, the cable will operate correctly but the diagnostic features won't be available.

TD+/TD- are mandatory and are used for the upstream link to the EP device. This differential pair must be connected to the dedicated transmitter pins of the FPGA (MGTPTX, MGTXTX or MGTHTX). It is recommended to place AC coupling capacitors on the target system as close as possible to the FPGA pins.
At least one RD+/RD- is mandatory. One of them is used per transceiver quad for the downstream link from the EP device.

If multiple SFP/SFP+ links are used, a single downstream link is required. The *RD+/RD-* differential pair must be connected to the dedicated receiver pins of the FPGA (MGTPRX, MGTXRX or MGTHRX). AC coupling capacitors are placed in the EP devices for the downstream links and hence no AC coupling capacitor is required for the receiver lines on the target system.

The control and status signals of the SPF/SFP+ connector, are not mandatory. Connecting these pins to an FPGA bank compatible with +3.3V IO signalling allows using the diagnostic features of the IP embedded in the target FPGA. These pins are not required for the IP operation. Table 2 describes how to connect these pins if the diagnostic feature is not used. The IP diagnostic feature gives the possibility to automatically detect the module or cable presence, to read the module or the cable identification, and so on.

If multiple SFP/SFP+ links are used, it is possible to spare FPGA pins by connecting the corresponding control and status lines of modules together.

Note: *The I²C bus of multiple SFP/SFP+ links cannot be connected together to form a single bus. All modules have the same I²C slave address. Placing several modules on the same bus will create conflicts. One I²C (SDA/SCL) pair must be used per SFP/SFP+ links. An I²C bus switch component can be added on board to reduce the number of used FPGA user IO.*

Table 2: Handling unused SFP/SFP+ control and status signals.

Pin #	Signal	Description
2	TX Fault	Keep unconnected when not used.
3	TX Disable	Must be connected to GND to enable the module by default.
4	MOD-DEF2	Pull-up to +3.3V.
5	MOD_DEF1	Pull-up to +3.3V.
6	MOD-DEF0	Keep unconnected when not used
7	RS0	This pin has no effect for passive cables. Pull-up resistor of maximum 10K is recommended (check optical module manufacturer documents for more details).
8	LOS	Keep unconnected if not used.
9	RS1	This pin has no effect for passive cables. Pull-up resistor of maximum 10K is recommended (check optical module manufacturer documents for more details).

QSFP28 Cage

The new version of the Exostiv Labs EP probe is equipped with a QSFP28 connector. The standardized pinout (refer to Figure 2) is respected so the probe is compatible with any standard QSFP/QSFP+/QSFP28 passive cable and/or active optical modules.

This connector guarantees the compatibility of the new probe revision with the boards interfaced with the previous version of the probe as standard breakout cables exist to connect a single QSPF28 cage to up to 4 SFP/SFP+/SFP28 cages.

To connect the Exostiv Labs EP probe to your target board, using the QSFP28 connector, the board must be equipped with one of the following connectors:

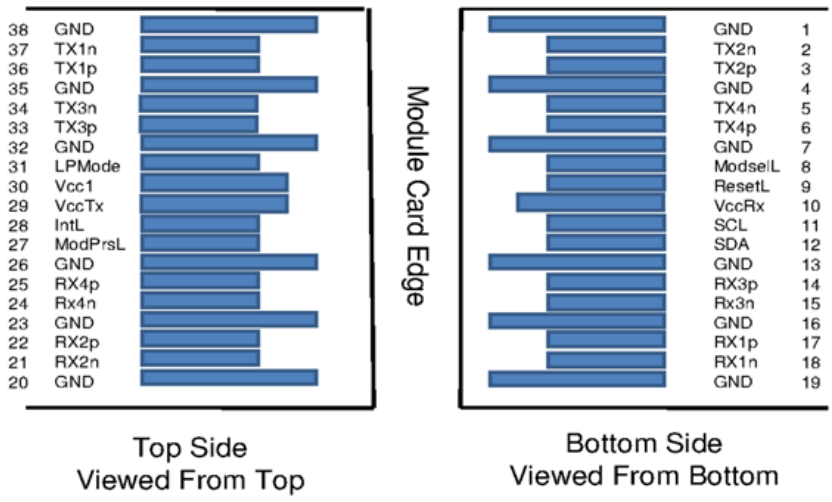
1. QSFP/QSFP+/QSFP28 (all with compatible pinout).

2. QSFP-DD (using standard breakout cable QSFP-DD to 2xQSFP28).
3. SFP/SFP+/SFP28 (using standard breakout cable QSFP28 to 4xSFP28).

In general, commercial boards equipped with these connectors have respected the standardized pinout and are ready to be used with any revision of the Exostiv Labs probe.
If you design your own board, and if you want to connect your board through the QSFP28 connector of the probe, you must respect the following rules:

1. Respect the standardized pinout of the selected connector.
2. If you intend to only use passive cables to interconnect the probe and the board, you do not have to connect the power and control pins to your board. They can remain unconnected. In this case, only the GND pins, TX and RX pairs must be connected to the board. With this configuration it is not possible to use active optical modules.
3. It is allowed to do some pin swapping under the following restrictions:
    a. Polarity can be inverted within any TX or RX pair, independently of any other pair. This means that the position of the P and N pins within any pair can be swapped if required. The probe will automatically detect the pin swap and invert the stream polarity internally.
    b. Respect the TX and RX pair relative positions. This means that when connecting any FPGA transceiver channel to the connector, if the RX pair of the FPGA channel is connected to pair RX*i* on the connector (with *i* = 1,2,3 or 4), then the FPGA TX channel must be connected to pair TX*i* on the connector. There is no required mapping between the FPGA bank channel indexes and the connector pair indexes.

Figure 2: QSFP28 standardized pinout



Important Note : *The Exostiv Labs IP can be configured to use up to 4 transceiver channels for the communication link. All the channels used in the link must be in the same FPGA transceiver bank. It is not allowed to split the IP link over several transceiver banks. When you design your board, make sure that all transceiver pairs connected to the connector(s) selected to interface the Exostiv Labs probe are issued from the same bank.*

ARF6-08

The ARF6-08 connector of the latest revision of the Exostiv Labs probe is the new high-density connection solution to interface your board.
With this connector you can interface your board at the full probe speed with a reduced PCB area. Depending on the chosen target connector configuration, the reserved area on your PCB to benefit of the Exostiv Labs features can be as small as 0.8 cm² (0.124 in²).

The ARF6-08 connector present on the Exostiv Labs probe is a standard product of SAMTEC company. Refer to the company web site for a complete description of the connector.
The Exostiv Labs probe is equipped with the right-angled version of the connector, ARF6-08-RA. The user is free to select the vertical or right-angled version of the connector on its target board.

Figure 3: Horizontal (right-angled) and vertical versions of ARF6-08 connector

Except the form factor, there is no difference between these two connectors. They both have the same pinout and are compatible with the Exostiv Labs probe. The user should base its choice only on the mechanical constraint of its board.

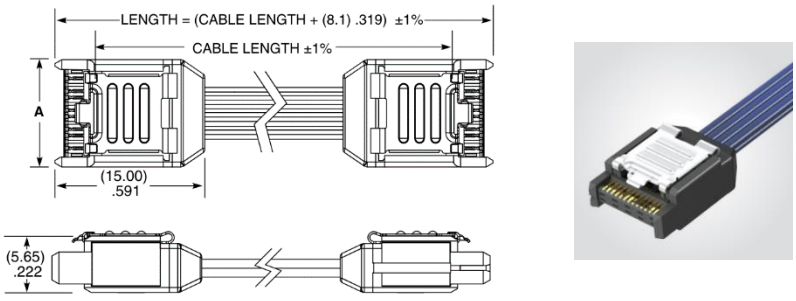
The ARF6-08 connector has been selected for its high bandwidth (up to 32 Gbps) and its capacity of routing 8 differential pairs with a reduced size. With this small form factor connector, it is possible to implement a reliable link with up to 4 transceiver channels at the full probe bandwidth.

Table 3: ARF6-08 connector features.

Part Number	Orientation	Area cm² (in²)	Dimensions (WxLxH) mm	Dimensions (WxLxH) inch
ARF6-08-S-D-A-K-TR	Vertical	0.79 (0.122)	11.82 x 6.7 x 13.95	0.465 x 0.264 x 0.549
ARF6-08-S-RA-TR	Horizontal (right-angled)	1.65 (0.255)	12.46 x 13.24 x 7.61	0.490 x 0.521 x 0.299

The pinout of the connector has been selected to be compatible with the standard SAMTEC high speed ARC6-08 and FQSFP cables. The ARC6-08 cable is used to interconnect two ARF6-08 connectors to each other. If the target board is equipped with an ARF6-08 connector, this type of cable must be used to connect the Exostiv Labs to the target board (refer to Figure 4). The pinout is provided in Table 4. For a detailed mechanical description of the connector, refer to the SAMTEC documentation.

Figure 4: High-speed ARC6-08 cable



We recommend using the ARC6 cable with following part number to interconnect the target board and the Exostiv Labs probe: ARC6-08-XX.X-LU-LD-2-1

With XX.X representing the total cable length in inch. For example, for a 15 inches cable length, the part number is ARC6-08-15.0-LU-LD-2-1

Table 4: ARF6-08 connector pinout on target board.

Name	Pin	Pin	Name
GND	1	2	GND
RX1n	3	4	TX4p
RX1p	5	6	TX4n
GND	7	8	GND
RX3n	9	10	TX2p
RX3p	11	12	TX2n
GND	13	14	GND
RX2n	15	16	TX3p
RX2p	17	18	TX3n
GND	19	20	GND
RX4n	21	22	TX1p
RX4p	23	24	TX1n
GND	25	26	GND

When connecting the FPGA transceiver bank to the ARF6-08 connector, the following rules must be followed:

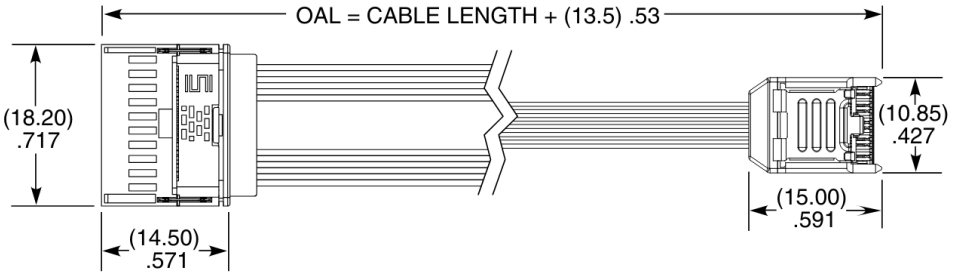
1. Respect GND pins position defined in Table 4.
2. Respect the TX and RX pair relative positions.
3. Pin swap within any TX or RX pair is allowed. This means that the P and N signals can be swapped within any pair.

Rule 2 means that when connecting an FPGA transceiver channel to the connector, if the RX pair of the FPGA channel is connected to pair RX*i* on the connector (with *i* = 1,2,3 or 4), then the FPGA TX channel must be connected to pair TX*i* on the connector.

Important Note : *The Exostiv Labs IP can be configured to use up to 4 transceiver channels for the communication link. All the channels used in the link must be in the same FPGA transceiver bank. It is not allowed to split the IP link over several transceiver banks. When you design your board, make sure that all transceiver pairs connected to the connector(s) selected to interface the Exostiv Labs probe are issued from the same bank.*

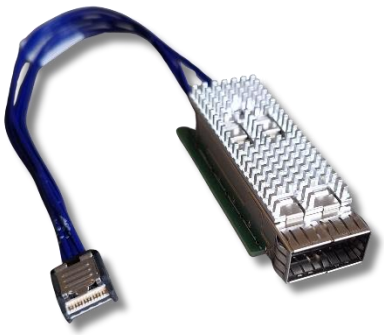
ARF6-08 to QSFP28 Adapter

As mentioned in the previous section, the ARF6-08 pinout has been chosen to also be compatible with FQSFP cable from SAMEC. This cable has on one end, an ARC6-08 connector to match the ARF6-08 connector placed on the target board; and on the other end, a QSFP28 receptacle. Refer to SAMTEC web site for a detailed description of the cable.



The FQSFP cable is part of the FLYOVER cable family from SAMTEC. The QSFP receptacle is supposed to be solder on a PCB to mount the QSFP cage around the receptable. Exostiv Labs has developed an adapter based on the FQSFP cable.

Figure 5: FQSFP to ARC6 adapter



This adapter gives the possibility to connect the previous version of the EP probe to a target board equipped with ARF6-08 connector. To do so, the ARC6-08 adapter must be used in conjunction with a standard QSFP+ to 4x SFP+ breakout cable.

This adapter also gives the possibility to connect the other Exostiv Labs products, such as the Exsotiv Blade, which only have QSFP28 connectors.

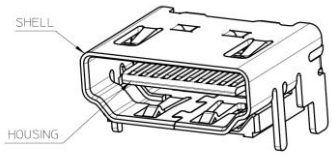
Other connectivity

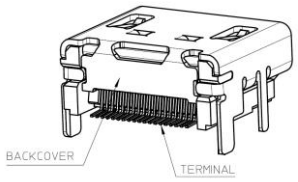
Should the connectivity solutions proposed in this document not be suitable for your needs, please contact Exostiv Labs to select a more suitable or compact connectivity. Exostiv Labs technical team can select the best available solution for your needs, with a readily available connector adapter or advanced cable assemblies.

HDMI Connector (! Legacy section, do not use for new designs !)

Important Note : *It is not recommended to use this option as custom connector for new designs. The description that follows is provided for legacy support purposes. From the EP16000 series probe, this connector* ***is not supported****. Consider using the ARF6-08 connector as replacement high-density connection option.*

The HDMI port is implemented using a 19-pin type-A HDMI compatible connector. Industry standard HDMI cables can be used to connect the EP devices to the user's target system. Table 5 provides some examples of compatible connectors that can be placed onto the target system board.





Even if the EP devices use a type-A HDMI connector, the target system can be equipped with space saving type-C (mini-HDMI) or type-D HDMI (micro-HDMI) connectors. In this case, a connector adapter or a cable with a different connector on each end must be used to connect the EP device to the target system. Using type-B induces the presence of via on the transceiver lines. With type-A connector, straight routing without via is possible.

Table 5: Examples of compatible HDMI connectors

Manufacturer	Part Number	Connector Type
Molex	047151-1001	Type-A
FCI	10029449-001RLF	Type-A
TE Connectivity	1747981-1	Type-A
CNC Tech	2000-1-2-30-00-BK	Type-A
Molex	046765-0001	Type-D
CNC Tech	2002-1-2-40-30-BK	Type-D

This list is not exhaustive.

Table 6 provides the pin assignments for type-A, type-C and type-D HDMI connectors. The HDMI interface uses up to 4 simplex multi-gigabit links from the target system to the EP device (upstream data flow direction). The differential GTX data lines must be connected to the dedicated transmitter pins of the FPGA (MGTPTX, MGTXTX or MGTHTX). It is recommended to place AC coupling capacitors on the target system as close as possible to the FPGA pins.

Table 6: HDMI Type-A and Type-D connector pin assignments

Type-A[(1)]	Type-C[(4)]	Type-D[(2)]	Signal	Description
1	2	3	T2Y_Data3+	Positive data line of the 4th GTX[1] differential pair from target system to EP device. Connect to MGTPTXP, MGTXTXP or MGTHTXP pin of the FPGA.
2	1	4	D3_Shield	Shield for 4th GTX differential pair
3	3	5	T2Y_Data3-	Negative data line of the 4th GTX differential pair from target system to EP device. Connect to MGTPTXN, MGTXTXN or MGTHTXN pin of the FPGA.
4	5	6	T2Y_Data2+	Positive data line of the 3rd GTX differential pair from target system to EP device. Connect to MGTPTXP, MGTXTXP or MGTHTXP pin of the FPGA.
5	4	7	D2_Shield	Shield for 3rd GTX differential pair
6	6	8	T2Y_Data2-	Negative data line of the 3rd GTX differential pair from target system to EP device. Connect to MGTPTXN, MGTXTXN or MGTHTXN pin of the FPGA.
7	8	9	T2Y_Data1+	Positive data line of the 2nd GTX differential pair from target system to EP device. Connect to MGTPTXP, MGTXTXP or MGTHTXP pin of the FPGA.
8	7	10	D1_Shield	Shield for 2nd GTX differential pair
9	9	11	T2Y_Data1-	Negative data line of the 2nd GTX differential pair from target system to EP device. Connect to MGTPTXN, MGTXTXN or MGTHTXN pin of the FPGA.
10	11	12	T2Y_Data0+	Positive data line of the 1st GTX differential pair from target system to EP device. Connect to MGTPTXP, MGTXTXP or MGTHTXP pin of the FPGA.
11	10	13	D0_Shield	Shield for 1st GTX differential pair
12	12	14	T2Y_Data0-	Negative data line of the 1st GTX differential pair from target system to EP device. Connect to MGTPTXN, MGTXTXN or MGTHTXN pin of the FPGA.
13	13	15	DNC	Do not connect. Keep this pin floating.
14	14	2	DNC	Do not connect. Keep this pin floating.
15	15	17	Y2T_SCL	I²C serial clock from EP to target system. EP device is the I²C bus master. Add 2KΩ pull-up resistor on target system. Connect this pin to an FPGA user IO.
16	16	18	Y2T_SDA	I²C serial bi-directional data line. Add 2KΩ pull-up resistor on target system. Connect this pin to an FPGA user IO.
17	17	16	GND	Reference signal ground
18	18	19	DNC	Do not connect. Keep this pin floating.
19	19	1	Presence Detect	Target presence detection. Connect this pin to signal ground.

[1] Tested with 10 m cable up to 6.6 Gbps per link and with 2 m cable up to 10.0 Gbps.
[2] Tested with 2 m cable up to 10.0 Gbps per link. Higher bit rates tests underway Please contact us for details.
[3] Transceiver + and – signals can be swapped within a differential pair if it is required to improve the layout. The EP can dynamically invert the polarity of the received signals.
[4] Not tested yet – provided 'as is'.

When using the HDMI connector, the downstream communication (from the EP device to the target system) is implemented with the dedicated I²C serial bus of the HDMI connector. This link is used to control the IP that is embedded in the FPGA fabric. The EP device operates as the bus master and the target system as the slave. SCL and SDA lines must be connected to user IO pins of the FPGA; in

[1] GTX = 'Gigabit transceiver' or 'transceiver'. The abbreviation can change according to the FPGA vendor and FPGA family. In this document 'GTX' is used as a generic term.

addition, external pull-up resistors connecting SCL and SDA to a voltage reference from +2.5V to +3.3V must be added. If this voltage level range is not compatible with the selected FPGA bank, an I²C bus level converter must be inserted between the HDMI connector and the FPGA.

Table 7: I²C bus specifications through HDMI connector

Parameter		Min	Typ	Max	Unit
Voltage reference	V_{REF}	2.5V	-	3.3V	V
SCL/SDA pull-up resistor	-	-	2	-	kΩ
SCL/SDA voltage level (input to EP)					
Low-level	V_{IL}	-0.5	-	0.85	V
High-level	V_{IH}	2.31	-	6	V
Low-level output current	I_{OL}	3	9	-	mA

Note: *Even if an industry standard HDMI connector is used on EP series, do not connect any HDMI-compatible device. The multi-gigabit transceiver port **is not** pin and functionality-compatible with the HDMI video standard.*

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